

Rule 1.1/26

CLMPTO

10/20/03

tb

1. (currently amended) A programmable logic device (PLD)
comprising:

[input/output (I/O) interface having a first plurality of I/O register blocks, the first plurality of I/O register blocks being partitioned into a second plurality of I/O sections each I/O section having N data I/O register blocks and a strobe circuit, wherein each of the N data I/O register blocks is configured to store multiple bits of data, and each strobe circuit is configured to generate a local strobe signal that drives a local clock line coupling to clock inputs of the N data I/O register blocks, the N data I/O register blocks and the strobe circuit in each I/O section being coupled to a corresponding number of device pins; and

programmable logic circuitry coupled to the I/O interface]

an interface module including:

a plurality of register blocks each having a data input coupled to a respective data pin and a clock input couple to a clock network, each register block having at least two registers, and

a strobe circuit having a strobe input coupled to receive an input strobe signal, a control input coupled to receive a phase control signal, and an output coupled to the clock network;

phase control circuitry coupled to receive an input clock signal and configured to generate the phase control signal at an output; and

programmable logic circuitry coupled to the interface module, wherein the interface module and the programmable logic circuitry can be configured for multiple data rate operation.

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~~2~~. (new) The PLD of claim ¹⁷~~2~~ wherein the strobe circuit generates a local strobe signal by shifting a phase of the input strobe signal in response to the phase control signal.

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~~3~~. (new) The PLD of claim ¹⁷~~2~~ further comprising a plurality of interface modules grouped into one or more interface banks.

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~~4~~. (new) The PLD of claim ¹⁸~~3~~ wherein a separate phase control circuit is provided for each of the plurality of the interface modules.

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~~5~~. (new) The PLD of claim ¹⁸~~3~~ wherein a separate phase control circuit is provided for each interface bank.

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~~6~~. (new) The PLD of claim ¹⁸~~3~~ wherein one phase control circuit is provided for all interface banks.

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~~7~~. (new) The PLD of claim 1 wherein each register block comprises two registers, one of which stores a first incoming bit of data at a rising edge of the local strobe signal and the other stores a second incoming bit of data at a falling edge of the local strobe signal.

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~~8~~. (new) The PLD of claim ¹⁷~~2~~ wherein the strobe circuit comprises a programmable phase delay circuit that is configured to adjust a phase delay of the local strobe signal such that an edge of the local strobe signal occurs substantially at the center of a data pulse.

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~~9~~. (new) The PLD of claim ²³~~8~~ wherein the phase delay is about 90 degrees.

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10. (new) The PLD of claim 1 wherein the interface module further comprises one or more general purpose register blocks coupled to respective device pins.

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11. (new) The PLD of claim 1 wherein the strobe circuit is located as close to a center of the plurality of data register blocks as possible wherein an equal number of data register blocks are located on either sides of the strobe circuit.

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12. (new) The PLD of claim 1 wherein the programmable logic circuitry comprises a plurality of programmable logic blocks coupled via a network of a plurality of programmable vertical and horizontal interconnect lines.

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13. (new) The PLD of claim 12 wherein each of the programmable logic blocks comprises look-up table logic.

²⁹ ²⁷
14. (new) The PLD of claim 12 wherein each of the programmable logic blocks comprises product term logic.

³⁰ ²⁷
15. (new) The PLD of claim 12 wherein each of the programmable logic blocks comprises a unit of programmable logic and a unit of memory.

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16. (new) A computing system comprising a multiple data rate memory circuit coupled to a programmable logic device (PLD) as set forth in claim 1.

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17. (new) The computing system of claim 16 wherein the multiple data rate memory circuit comprises a double data rate synchronous dynamic random access memory.

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18. (new) A method of operating a programmable logic device (PLD)

comprising:

receiving a plurality of data signals and an associated data strobe signal;

applying the plurality of data signals and the associated data strobe signal to a corresponding plurality of register blocks and strobe circuit, respectively;

generating a phase control signal in response to an input clock;

shifting a phase of the data strobe signal to generate a local strobe signal, in response to the phase control signal;

driving clock inputs of registers inside each register block using the local strobe signal; and

coupling the plurality of register blocks to programmable logic circuitry.

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19. (new) The method of claim 18 wherein the shifting of the phase of the data strobe signal can be programmably modified.

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20. (new) The method of claim 18 further comprising partitioning the plurality of register blocks into a plurality of N modules each module having M register blocks and one strobe circuit.

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21. (new) The method of claim 20 further comprising disposing the one strobe circuit in each module as close to a center of the M register blocks as possible wherein an equal number of register blocks are located on either sides of the strobe circuit.

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22. (new) The method of claim 18 wherein the shifting of the phase of the data strobe signal shifts the phase such that an edge of the local strobe signal occurs substantially at the center of a data signal pulse.